



ATTACHMENT 1(g)

LIST OF ADDITIONAL SUBMITTED DOCUMENTS	ATTORNEY DOCKET NO.	APPLICATION NO.
	1450.1035	10/686,638
	FIRST NAMED INVENTOR	
	Toshiaki SARUWATARI, et al.	
	FILING DATE	GROUP ART UNIT
	October 17, 2003	2181

The following document(s) is/are listed in accordance with the duty of disclosure provisions of 37 CFR § 1.56, so that the Examiner may consider same should he deem any thereof to be material to examination of the subject application.

It is requested that the Examiner acknowledge his consideration of document(s) below-listed by initialing same in the space provided adjacent each such application and that the Examiner sign and date this form at the bottom thereof to confirm such consideration having been given.

This submission in no way represents an admission that any of the information listed herein constitutes prior art with respect to the subject application; and unless and until such prior art status is established, this submission is not a request that the information presented herein be printed on the face of any patent issuing from the subject application in which this information is being filed.

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
	AA						
	AB						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION YES NO	
	AC							
	AD							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

						TRANSLATION YES NO	
<input checked="" type="checkbox"/>	AE	Copy of European Search Report dated May 17, 2006 for corresponding European Application No. 03256630.9.					

EXAMINER	<i>[Signature]</i>	DATE CONSIDERED	3-6-07
<p>*EXAMINER: Initial if document considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</p>			



Sheet 1 of 1

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTORNEY DOCKET NO.	APPLICATION NO.
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U.S. PATENT DOCUMENTS

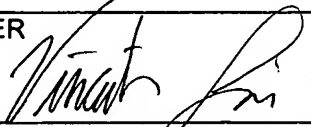
*EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
W	AA	4,722,050	1/26/1988	Lee et al.	364	200	3/27/1986

FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	TRANSLATION YES NO		ABSTRACT
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

				TRANSLATION YES NO	
	AM	Brown et al., "Implementing Sparc in ECL", IEEE Micro, Vol. 10, No. 1, 1 February 1990, pgs. 10-21.			
	AN	Katevenis et al., "Reducing the Branch Penalty by Rearranging Instructions in a Double-Width Memory", Computer Architecture News, Vol. 19, No. 2, 1 April 1991, pgs. 15-27.			
	AO	Ando, et al., "Speculative Execution and Reducing Branch Penalty on a Superscalar Processor", IEICE Transactions on Electronics, Vol. E76-C, No. 7, July 1993.			

EXAMINER 	DATE CONSIDERED 3-6-07
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